**IN THE CLAIMS:**

1. (Currently Amended) A cache controller used in a computer system that includes a cache memory, a main memory, and a microprocessor which concurrently executes a plurality of tasks, comprising:

a region managing unit operable to manage a plurality of regions in the cache memory in correspondence with the plurality of tasks;

an address receiving unit operable to receive, from the microprocessor, an address of a location in the main memory at which data to be accessed to execute one of the plurality of tasks is stored; [[and]]

a judging unit operable to judge whether the data stored at the received address is stored in the cache memory, by searching all of the plurality of regions in the cache memory; and

a caching unit operable to acquire, if the judging unit judges that the data ~~to be accessed~~ is not stored in the cache memory, a data block including the data from the main memory, and store the acquired data block into a region in the cache memory corresponding to the task.

2. (Original) The cache controller of Claim 1,

wherein the region managing unit divides the cache memory into the plurality of regions equal in number to the plurality of tasks, and manages the plurality of regions in a one-to-one correspondence with the plurality of tasks.

3. (Original) The cache controller of Claim 2,

wherein the region managing unit receives information about how many tasks are concurrently executed by the microprocessor and a size of memory required for execution of

each of the plurality of tasks, and divides the cache memory into the plurality of regions based on the received information.

4. (Original) The cache controller of Claim 3, further comprising:

a task ID receiving unit operable to receive a task ID of the task,

wherein the region managing unit manages the plurality of regions in a one-to-one correspondence with task IDs of the plurality of tasks, and

the caching unit stores the acquired data block into the region in the cache memory corresponding to the received task ID.

5. (Original) The cache controller of Claim 4,

wherein the task ID is an address of a location in the main memory at which the task is stored as a program.

6. (Original) The cache controller of Claim 4,

wherein the task ID is generated by converting an address of a location in the main memory at which the task is stored as a program.

7. (Original) The cache controller of Claim 4,

wherein the microprocessor performs multitasking under control of an operating system, and

the task ID is a process ID assigned by the operating system.

8.-9. (Cancelled)

10. (Original) The cache controller of Claim 4,

wherein the cache memory is made up of a plurality of ways, and

the plurality of regions each contain at least one way.

11. (Original) The cache controller of Claim 10, using set associative mapping for each region containing more than one way.

12. (Original) The cache controller of Claim 1,

wherein the region managing unit divides the cache memory into a specific region and a nonspecific region, and manages the specific region in correspondence with a specific task out of the plurality of tasks, and

the caching unit stores the acquired data block into the specific region if the task is the specific task, and into the nonspecific region if the task is other than the specific task.

13. (Original) The cache controller of Claim 1,

wherein the microprocessor concurrently executes a first task, a second task, and a third task,

the region managing unit divides the cache memory into a first region and a second region, and manages the first region in correspondence with the first task and the second task, and the second region in correspondence with the third task, and

the caching unit stores the acquired data block into the first region if the task is the first task or the second task, and into the second region if the task is the third task.

14. (Currently Amended) A cache control method used in a computer system that includes a cache memory, a main memory, and a microprocessor which concurrently executes a plurality of tasks, comprising:

a region managing step of managing a plurality of regions in the cache memory in correspondence with the plurality of tasks;

an address receiving step of receiving, from the microprocessor, an address of a location in the main memory at which data to be accessed to execute one of the plurality of tasks is stored; [[and]]

a judging step of judging whether the data stored at the received address is stored in the cache memory, by searching all of the plurality of regions in the cache memory; and

a caching step of acquiring, if the judging step judges that the data ~~to be accessed~~ is not stored in the cache memory, a data block including the data from the main memory, and storing the acquired data block into a region in the cache memory corresponding to the task.

15. (Currently Amended) A computer system comprising a cache memory, a cache controller, a main memory, and a microprocessor which concurrently executes a plurality of tasks, the cache controller including:

a region managing unit operable to manage a plurality of regions in the cache memory in correspondence with the plurality of tasks;

an address receiving unit operable to receive, from the microprocessor, an address of a location in the main memory at which data to be accessed to execute one of the plurality of tasks is stored; [[and]]

a judging unit operable to judge whether the data stored at the received address is stored in the cache memory, by searching all of the plurality of regions in the cache memory; and

a caching unit operable to acquire, if the judging unit judges that the data ~~to be accessed~~ is not stored in the cache memory, a data block including the data from the main memory, and store the acquired data block into a region in the cache memory corresponding to the task.

16. (Original) The computer system of Claim 15, further comprising:

an address converting unit operable to receive from the microprocessor a logical address showing the address of the location in the main memory at which the data to be accessed is stored, convert the logical address to a physical address, and send the physical address to the address receiving unit,

wherein the cache controller further includes:

a data block managing unit operable to manage the data block stored in the cache memory by the caching unit, using the physical address.

17. (Original) The computer system of Claim 15,

wherein the address receiving unit receives from the microprocessor a logical address showing the address of the location in the main memory at which the data to be accessed is stored,

the cache controller further includes:

a data block managing unit operable to manage the data block stored in the cache memory by the caching unit, using the logical address, and

the computer system further comprises:

an address converting unit operable to convert the logical address output from the cache controller to a physical address, and send the physical address to the main memory.